Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **PCPOUT**
2. **PC1OUT**
3. **COMPIN**
4. **VCOOUT**
5. **INH**
6. **C1A**
7. **C1B**
8. **GND**
9. **VCOIN**
10. **DEMOUT**
11. **R1**
12. **R2**
13. **PC2OUT**
14. **SIGIN**
15. **PC3OUT**
16. **VCC**

**.064”**

**.078”**

**11 10 9 8 7 6**

**12**

**13**

**14**

**5**

**4**

**3**

**15 16 1 2**

**HC**

**4046AT**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: N/C**

**Mask Ref: HC4046AT**

**APPROVED BY: DK DIE SIZE .064” X .078” DATE: 1/26/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54HC4046A**

**DG 10.1.2**

#### Rev B, 7/1